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Transmitter Protection System

TPS02

Operating Manual

generic sales/info version, 10/29/18

Contents

1.0 Legalities

1.1 Warranty & Disclaimer

The provided equipment is scientific instrumentation. The success or failure of its use depends as much on the integration by the user as on the design and fabrication by the manufacturer. Improper installation or operation can result in equipment failure and/or personal injury. The user accepts responsibility to read and understand provided manuals, and to ensure safe operation of the installation where it is used. This manual is written to aid the skilled system integrator through the setup and installation of the instrumentation.

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1.2 Notice of Proprietary Schematics and Source Code

The schematics and firmware source code are generally provided as support materials along with transmitter protection systems – however an NDA must be executed with the agreement that these materials are for support, not for reprocurement nor reverse engineering.

1.3 Manual Date and Version

This edit of the TPS02 manual is for generic sales/information purposes, and any customer specific implementation data has been omitted. Last edit was 10/29/18.

2.0 Introduction

The TPS02 is packaged with several accessories – be sure that these are all accounted for when unpacking:

- The TPS02 main unit – a rack-mount chassis with an impressive number of connectors.

- The TPS02 may optionally be provided with ball-bearing sliding rail travelers mounted to the chassis sides. When supplied, the mounting brackets are enclosed separately. These are adjustable from 24" to 30" to accommodate the mounting rails in your rack.

- AC line cord. See Section 4.5.1.

- Interlock jumper (installed), with spare connector & pins packaged separately.

- Documentation CD and hardcopy manual.

- USB Cable. **(Warning – the USB cable is not to be left connecting the TPS02 to an external computer while operating. Most operating systems cycle the USB initialization on *all* USB ports when any USB device is plugged in, as well as at other times. This init sequence *will* reboot the TPS02, with unpredictable results. Only connect the USB when doing maintenance to reprogram the internal firmware, and only after putting connected equipment in "safe" condition.)**

3.0 Quick Start

There is no quick start. You are trying to protect an expensive klystron. Many connections to diagnostics and PLC controls are necessary to engage TPS02 functions. Pour a big cup of coffee and understand the manual thoroughly.

Minimal interconnections required are:

- Diagnostics (current transformers, shunts, arc detectors) to specified rear panel BNCs,

- Inputs for HV and RF pulse requests on rear panel (alternate – use internal pulse generator mode),

- control signal inputs from PLC or switch panel, *via* SCSI-68 rear panel connector,

- HV command pulse output to modulator and RF command pulse output to RF switches, *via* rear panel BNC outputs,

- AC line power,

- Do NOT hookup USB cable. This is for maintenance / reprogramming only. Leaving USB connected may cause spurious reboots at unwanted times, disabling the TPS02.

4.0 Overview

The TPS02 was originally designed to meet one customer's specifications for transmitter protection on a high power klystron. The design, however, is modular and easily reconfigurable. As originally designed, the basic description for the TPS02 (36 channel) is:

- A single rack-mount 3U chassis, providing analog processing for 36 signals, plus a number of control & status digital signals,
- Fast fault detection using 45ns comparators and programmed logic matrices for latching and inhibiting pulsing when faulted,
- On-board CPU control of remotely settable comparator thresholds, inhibit timing delays, event logging, and test-function local pulse generation,
- Ergonomic features, including front panel LCD and rotary encoder for local displays and some settings; front panel monitor testpoints (BNC) for all analog channels, and LED fault indicators, and serial port for remote communications.

4.1 Options

The TPS02 comprises two types of circuit boards – control and analog. The TPS02 (36 channel) as described through most of this manual uses one control and two analog boards. The control board services all system I/O, fast logic, and service for four analog channels. Each analog board services an additional 16 analog channels, and is slaved to the control board.

Other custom options can be configured: a TPS02 (4 channel) using only a single control board, a TPS02 (20 channel) using one control board and one analog board, a TPS02 (52 channel) using a control board and three analog boards, etc. It is also possible to configure a single analog board as a TPS02 with reduced control capabilities, although the 16 channel analog capability would be reduced by reallocating several analog channels for digital I/O.

All further discussion will address the standard TPS02 (36 channel) configuration.

4.2 Physical Topology

The TPS02 is implemented in three circuit boards, stacked in a 3U chassis, each approx 15"x10". Two of these boards are of the same design – "analog" boards which do the bulk of the signal processing, and are slaves to the control board discussed below. Each analog board does all analog processing for 16 channels and little else.

Each analog board is controlled by two programmable chips – a 10ns programmable logic array CPLD[1] (Atmel ATF1508) and an ARM7 32-bit CPU. The CPU manages setup and interrogation I/O tasks, and the CPLD manages all fault latches and fault logic pathways. The two analog boards run the same code in the CPU, but each has separately configured CPLD code.

[1] CPLD: Complex Programmable Logic Device. This is an acronym used for programmable logic chips which are bigger than PALs and smaller than FPGAs.

The top board is a "control" board, which processes four analog signals with additional instrumentation, plus manages all controls and communication. It is somewhat reconfigurable as well. It has three programmable chips – two 10ns CPLDs (one largely for fault latches, the other for control logic), and a larger variant of an ARM7 CPU. All of the user ergonomics are coded in this CPU.

4.3 Design Topology

The primary purpose of the TPS02 is to protect the klystron from damage – from tube arcs, from waveguide arcs, or from accidental driving beyond the specified power limits. The functions of the TPS02 which provide this protection are designed to be rugged and reliable. The critical signal pathways for this protection are entirely within the programmed logic (CPLD) chips.

The TPS02 has, by specification, a number of more *poetic and ergonomic* features which serve as convenience to the operators. Despite being embedded in the same box, these features are largely independent, and present *requests* to the frontline gauntlet of logic permissives which serve to protect the klystron.

4.3.1 Analog Systems

The bulk of the TPS02 comprises 36 analog channels[2], each represented by the block diagram at right. The design is general with many configuration options, and each channel will be pre-configured per the customer specifications. Configuration differences primarily lie in the initial signal scaling (gain, offset, polarity) and in the number and configuration of fault comparators. Note that all analog channels have the inputs on the rear panel and only the monitor testpoints on the front panel. There are no analog inputs on the front panel.

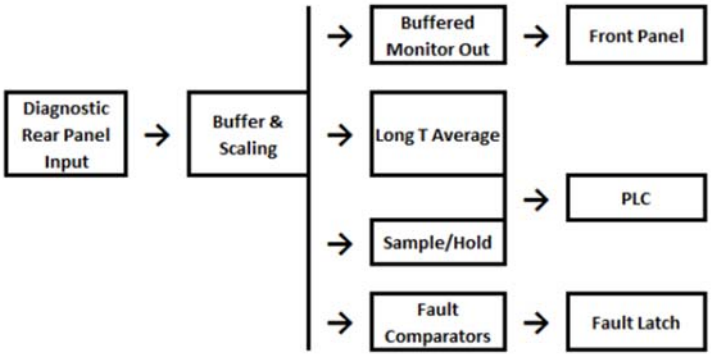


Figure 1. Block Diagram of one analog channel.

[2] 36 channels for a 3U system with two analog boards. The actual analog signal count is 16 per analog board, plus another 4 on the control board.

4.3.2 Fault Logic

The authority of the TPS02 to protect the klystron lies in blocking the pulse requests from passing through to the HV modulator or to the RF switches. This permissive logic combines the fault latches, the pulse requests, and several system state bits to enable or disable output pulsing.

It is important to note that this gauntlet of permissive logic lies *entirely* in the fast programmable logic devices (CPLDs). The fault response does not rely on the CPU (with its slower response and far more complex firmware).

There are cases where the CPU can, through setting of state variables, instruct the CPLDs to block output pulsing, but the CPU cannot override the CPLD logic to force pass-through of pulsing when fault logic should forbid it.

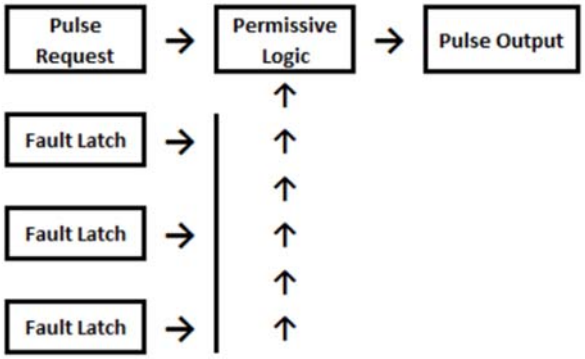


Figure 2. Block Diagram of fault logic permitting pulse pass-thru.

4.3.3 Ergonomic Features

As a convenience to the transmitter operator, a number of extra features are provided – these *lie on top* of the topology discussed above, i.e. they sample, display, communicate, calibrate, and aid in setting parameters – but they do not lie in the fault permission path.

Communications: For setup of adjustable parameters, the user has a choice of both a remote serial port and a front panel LCD display & rotary encoder interface. Parameters selected are saved in non-volatile memory for stability across power-up cycles.

LCD Monitor: For monitoring from the transmitter room, the LCD display has a selection of top-level monitors, which display sample/hold values of key diagnostics, calibrated and displayed with appropriate units.

Pulse Generator: For operating independently of the radar controls (i.e. tube conditioning or testing), the TPS02 has a highly configurable internal pulse generator.

Event Logging: For inspecting the sequence of events leading to a fault condition, the TPS02 has an internal event logger, which tracks up to 48 bits (fault and status bits) and saves a snapshot of all 48 plus a timestamp whenever any of them change. These events are saved in a cyclical buffer 4096 events deep. Unloading and inspecting this log after a fault will show the order of events and help specify potential collateral damage.

Odometer: For tracking the tube lifetime and duplexer lifetime, the cumulative history of the TPS02 is tracked several ways (time, integrated tube charge, integrated RF power). There

are two user accessible resets for re-zeroing the odometer when mounting a new klystron or a new duplexer.

RF Power Checks: Two methods have been installed to make comparisons between the beam power and RF power, and to alert the transmitter operator should they not reconcile. One of these is calculated in the CPU using the diode calibration curves, the other implemented entirely in hardware assuming a linear diode calibration curve. These are typically configured only as warnings, without authority to interrupt pulsing or latch the fault condition.

4.4 Tour – Front Panel

Figure 3. TPS02 Front Panel

The 3U, dual-analog-board TPS02 Front panel consists of 38 BNC outputs, a display with rotary encoder, an array of fault LEDs, an ESTOP button, a fault reset button, and a single-shot pushbutton. The LEDs have a group clustered on one corner for system status and faults, plus selected fault LEDs adjacent to signal monitor points associated with those signals.

4.4.1 Analog Monitors

The Analog Monitor points are buffered outputs of the internally buffered and scaled analog signals. These signals are typically current transformers, current shunts, voltage dividers, auxiliary HV power supply and/or modulator monitors, RF detectors, and spares. The output drivers are high bandwidth op-amps to optimize signal risetime, and the outputs are isolated with 453Ω series. Scalings are generally such to bring the expected signals to the positive 0-10V range.

4.4.2 Digital Monitors

The front panel also has three digital outputs, intended for synchronizing transmitter room diagnostics (i.e. scope triggering). These are redundant with identical signals present on the rear panel – the difference being that the rear panel signals are intended to be wired into the system controls, while the front panel signals are intended to be free for occasional transmitter room diagnostic use. These signals are HV and RF (echos of the control gate outputs), and FLT (fault). These digital outputs are buffered independently for front and rear panels. The outputs are driven by fast 1.5A digital buffers and include 50Ω series.

4.4.3 Signal FAULT and FIRST-LATCHED-FAULT LEDs

Fault LEDs accompany many of the monitor BNCs where the referred signal is internally wired to fault comparators. For most of these, there are two fault LEDs. One shows the status of the fault latch (faults latched must be reset in "people time" by the front panel pushbutton or the PLC). The other shows the "first-latched-fault" indication. Often, a single fault event triggers many others as the system shuts down, making diagnosis of root cause difficult. The fault logic grabs a "lockout" bus whenever any of the fault latches fires, and any faults that fire before this lockout bus is activated will also latch the "first-latch-fault" indication. This is not foolproof, as the fault events must be separated by the logic path latency and transmission time between boards (tens of ns), so it is possible for more than one signal to display "first" status.

Four of the analog signals in the TPS02 have additional instrumentation[3], which includes sensitivity to "interpulse" faults – faults where current or voltage is detected when the TPS02 is not gating a pulse. These signals have an additional LED for display of interpulse faults.

4.4.4 System Status and Fault LEDs

The upper right corner of the front panel has a tight cluster of additional LEDs. These include:

Waveguide Arcs – There are five channels of waveguide arc detection. Six LEDs show the latches for these plus a single "first-latched-fault" for the group.

Emergency STOP (ESTOP) – The front-panel emergency-stop button will kill TPS02 HV and RF gating outputs, as well other system controls as configured (such as communication to PLC to open facility breakers). This is both mechanically latched and electronically latched, and the LED shows the status of the internal latch.

INTERLOCK – The rear-panel interlock loop, if broken, has identical consequences to the ESTOP. A separate LED shows the status of this latch.

POWER FAULT – Each of the three boards in the TPS02 monitors several power supply rails, and declares a fault if any vary outside of acceptable ranges. This is indicated with the PFLT latch and the associated LED.

PLSERR – This is a non-interrupting warning indicator, showing that the external pulse train exceeds the specifications for the transmitter (for rep rate, pulsewidth, duty fraction, dead time,

[3] These are the four analog signals configured in the control board analog channels.

etc.). The pulse train is typically not halted, but pulses are truncated or omitted to bring the operation of the transmitter into compliance with the user specification.

SEQERR – This LED indicates a fault in the sequence of state operations, as configured. The particular configuration chosen will work with facility controls (such as external PLC) to sequence startup and shutdown, and this fault indicates a procedural failure.

RF ON – This LED is on whenever the TPS is gating the RF output signal to drive the system RF input to the klystron. This LED will appear on while pulsing at moderate to high rep rate, with brightness dependent on duty fraction.

HV ON – This LED is on whenever the TPS is gating the HV (beam) output signal to drive the HV modulator. This LED will appear on while pulsing at moderate to high rep rate, with brightness dependent on duty fraction.

Enabled – This LED is on when the TPS02 is enabled for pulsing, and pulse requests will be passed through to the output.

Power – This is lit whenever power is applied.

(prog) – This LED is lit whenever the TPS is being reprogrammed. Obviously, this should only be done when the transmitter is appropriately "safed".

HB – The TPS02 generates a "heartbeat" and passes it through all programmable chips. For CPUs (of which there are 3), the "pass through" occurs at the outermost polling level, not within an interrupt...thus guaranteeing that pass through will fail on any hangup. This should be flashing at about 2 Hz (it is toggled every 256 ms). It is tested internally, and both RF and HV outputs are locked out – with no possible override by any programmable chip – if it stops pulsing. The raw heartbeat is also passed externally to a PLC, which should be performing similar checks.

Local Pulsegen – The PLC may enable the TPS02 to generate pulse trains for testing, independent of the external drives normally used. If this enable bit is on, this LED is lit as an indicator / warning.

SFLT – This is a "soft fault" indicator – optional, available when certain faults, such as high RF reflected power, are to only shut down RF, perhaps with automatic retries after a designated delay.

HFLT – This is the "hard fault" indicator. This is generally indicative of an overcurrent due to a tube arc, requiring termination of both the RF and HV gate and requiring a manual reset.

XFLT – This shows an optional "extreme" fault. These are typically faults which require system facilities to open breakers to high voltage systems. Only the most severe faults call for this – such as ESTOP, interlock failure, or interpulse currents.

Comm – This LED shows activity on the serial port.

Spares – The system was designed with several additional LEDs, configurable as needed for the customer application.

4.5 Tour – Rear Panel

Figure 4. TPS02 Rear Panel.

The dense matrix of 54 BNC connections on the rear panel includes all of the analog inputs, digital fault inputs (waveguide arcs and external HV system faults), control signals, and selected digital outputs. Additional rear I/O includes the PLC interface, serial interface, differential TTL inputs for remote pulsing, external interlock, USB ports, and power entry.

4.5.1 Power Entry and Fusing

Supply power to the TPS with the provided IEC AC power cable. The only direct load is a commercial 5V 75W power supply, which has nameplate ratings of 100-240 VAC and 1.6A. In practice, the guts of the TPS02 typically draw only 4A of this 5V supply (i.e. 20W).

Power is filtered with the IEC power entry module *and* a Corcom 2-stage line filter. The power entry module has an on/off switch.

There is an in-line 1A fuse between power entry and the 5V power supply, and there is a slow-blow 5A surface-mount fuse on each of the three boards at the 5V power-entry. A high-current Schottky diode across the 5V power entry on each board ensures that reversing the power supply will blow this fuse before damaging components.

An internal fan may be added if desired, but is generally not necessary.

4.5.2 PLC I/O

Each of the (three) circuit boards in the TPS02 interfaces to the PLC via a SCSI 68 pin connector. All the control inputs are through the top connector, to the control board – the other connectors manage monitor and status signals sent to the PLC. Pinouts are detailed in Section 13.0

4.5.3 USB Ports

Each of the three circuit boards in the TPS02 also has a USB port. This is *only* to be used for maintenance (i.e. reprogramming), and should not be connected during normal operation.

It is important to note that leaving the USB ports connected to a local computer may result in occasional rebooting of one or more of the CPUs – exercising of the handshake lines which drive the programming reboot controls is often done by Windows when other USB ports are enumerated, for example plugging a memory stick into another USB port. This is serious – *do not leave the USB ports connected.*

New in 2018 – the TPS02.2 boards allow all reprogramming to channel through the control board, eliminating USB ports to the analog boards, and simplifying reprogramming of any of the internal chips. Functionality of the TPS02 system is otherwise unchanged.

4.5.4 Pulse inputs

The external pulse requests for beam (HV) and RF are received on the rear panel of the TPS02. There is a Dsub15HD connector for receiving these *via* differential TTL – alternately they may be configured as single-ended logic input on BNC cables.

4.5.5 Serial I/O (fiber optic)

A serial port is provided for remote configuration and inquiries which are more complex than the PLC interface is capable of. This port uses two 5 MBaud ST type transmitter/receivers, for use multimode 62.5/125 µm fiber. Default serial communications are 115200 baud.

4.5.6 Interlock

An external interlock is provided. This is a 10mA current loop, galvanically isolated from the rest of the TPS02 circuitry. The TPS02 is shipped with a jumper plug in place – this should be left in place, or replaced with the user's interlock wiring. A break in the continuity of the interlock is a most insegrevious transgression, and will result in blockage of all HV and RF gate outputs[4]. (This is equivalent, in control terms, to activation of the "E-Stop" button on the front panel.)

Internally, this is driven by an isolated 5V 50mA Murata supply, and loaded with 400 Ω in series driving an opto-isolator.

4.5.7 Analog Inputs – CTs

A number of analog inputs to the TPS are likely to be current transformer inputs. Typically, these are configured for a Pearson type CT, with a known calibration into 50 Ω. These channels are internally terminated with 50 Ω, then buffered with a gain sufficient to bring the internal analog bus to a full scale range of 10V or a bit less. The CTs should be oriented to provide a positive signal to the TPS02 – a reversed CT should be specified to fault at approximately -5% of nominal full scale, and one fault comparator is typically dedicated to detect reversed CT.

[4] ...as well as lifting of permission to the PLC to close facility HV power breakers, or whatever other state control signals are specified.

Typically, there are three comparators in use for faults on each CT – one is the reverse-detect noted above, one is set to an absolute do-not-ever-exceed value (generally set 5% over the max signal, with a moderate filter time). These two comparators are never inhibited and always active. The third comparator is remotely settable using a DAC reference and a programmable inhibit time on HV leading edge, and has a faster filter time (typically half of above).

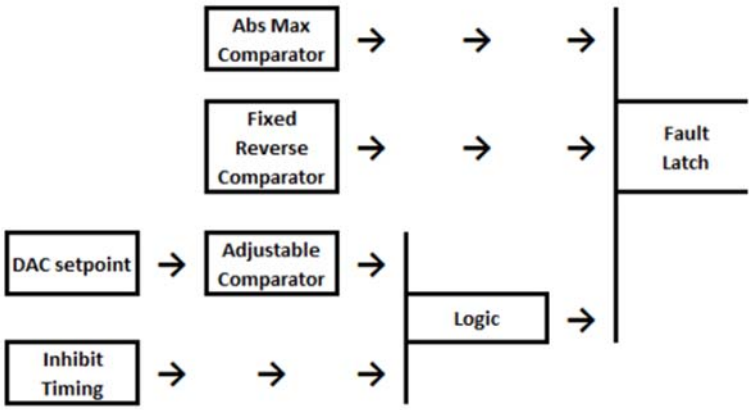


Figure 5. Block Diagram multiple comparators on a CT analog channel, including remotely programmable comparator threshold and inhibit timing.

The buffered and scaled internal analog signal bus feeds these comparators, as well as the monitor buffer for the front panel monitor, and a buffered average-current output to the PLC (using a slower *RC* time constant), plus a buffered S/H output to the PLC. (See Figure 1.)

One CT channel is typically brought in through one of the four control board analog channels thus has all this plus additional instrumentation[5]. The S/H output is also fed to a 12-bit ADC for internal calculations and for the front panel LCD display. There is also a *second* S/H channel which is gated when HV is *off* – the output of that S/H amp is filtered, then buffered and sent to the PLC. That same output is also sent to a comparator with a DAC reference for detecting interpulse faults.

The absolute do-not-ever-exceed values for all CT channels can be set with fixed resistors, or board-mounted trim-pots. Note that trim pots mounted on boards other than the top (control) board will be inaccessible without disassembly, and are thus not recommended.

4.5.8 Analog Inputs – Shunts

A TPS02 configuration may also include shunt current measurements. Typically, shunt currents require differential analog measurements, as "ground" is a dubious concept in high voltage pulsed power applications, and a return bus reference is needed to determine the voltage across the shunt accurately. Each analog board has optional differential amplifier circuits, appropriate for up to two such shunt signals per analog board (note that return-bus inputs must be allocated among the analog inputs on the same board). Typical implementation has two comparators dedicated to each differential output – fixed and DAC settable limits, but no reverse-detect.

4.5.9 Analog Inputs – Voltage Divider

One of the control board analog inputs is configured – dedicated, actually – to a high impedance compensated voltage divider. The design of this analog input precludes it from being scat-

[5] This channel is implemented on one of the four analog channels of the control board.

tered among the many other generally reconfigurable inputs. Different op-amps (low bias current), and other circuit configurations preclude this from being a general purpose channel. This channel is designated V_k (cathode voltage), and it is assumed that a commercial compensated divider (such as any of the Northstar or Ross dividers) will be used to provide the raw input – of negative polarity.

From here, much of the instrumentation is common with other signals: we have a buffered front panel monitor, a slow buffered average to the PLC, a S/H (gated by HV) to the PLC and to an ADC channel for calibrated display, and a second S/H (gated by not-HV) to the PLC and to an interpulse fault comparator with DAC reference. Analog overvoltage comparators and/or interpulse fault detect can be implemented. Should interpulse faults be implemented, a separate inhibit time channel should be used, as voltage fall time may be quite long in practice.

4.5.10 Analog Inputs – RF Diodes

A number of analog channels may be dedicated to RF diode signals. This number was quite large for the original TPS02 specification, but may be smaller or larger for future systems. These can be wired for either polarity diode inputs, and any scaling specified. Again, the internal analog bus will be scaled to have a typical dynamic range of approximately 0 to +10V.

For high power signals (i.e. klystron RF output path), these are typically in pairs from directional couplers, each having a forward and a reflected pair of signals. Typically, the forward power signals are minimally processed. The reflected power signals typically are assigned one fault comparator each, associated with a DAC reference fault threshold. Optionally, the analog boards have circuitry available to assign fault conditions to ratiometric detection, also using one DAC channel[6].

The TPS02 initial design specified that one pair of high power diode detectors (forward and reverse) were assigned to two of the four analog channels of the control board. This provides some additional instrumentation. In addition to the features above, the forward and reflected channels each have ADCs sampling the S/H output, as well as a second S/H interpulse (gated on not-RF) detect, with this S/H feeding a PLC signal and a comparator with DAC reference.

To make use of the forward and reflected power measurements attained with the ADC, we have provisions for entering calibration coefficients to convert the raw diode signal to a calibrated power.

4.5.11 Analog Inputs – HVPS and HVMOD monitors

Several options are provided to interface to the HV power system (power supply and/or modulator). Options exist to detect faults in those systems, and to echo analog monitor points from those systems. Details are implementation dependent.

[6] In ratiometric detection, a fault comparator triggers when the reflected voltage exceeds a fraction of the forward voltage. The fraction is specified by a DAC channel, using an analog multiplier, and a small offset is applied to prevent false triggers at zero power.

4.5.12 Digital Inputs

Additional digital inputs are provided on the rear panel, suitable for waveguide arc detection, or other system faults (such as those from power supplies or modulators). Impedance, polarity, and *RC* filter time can be customized. Input buffering uses Schmitt Trigger gates. A number of spare channels have circuit layouts for both inputs and outputs, and can be configured as needed.

4.5.13 Digital Outputs

A number of digital outputs are provided – generally providing the ultimate output gates (HV and RF) after passing the gauntlet of fault checks and permissives. These are buffered with 1.5A 45 ns logic level drivers with 50 Ω series. Fault monitoring, or other digital signals may be routed here as needed. A number of spare channels have circuit layouts for both inputs and outputs, and can be configured as needed.

5.0 LCD Display Interface

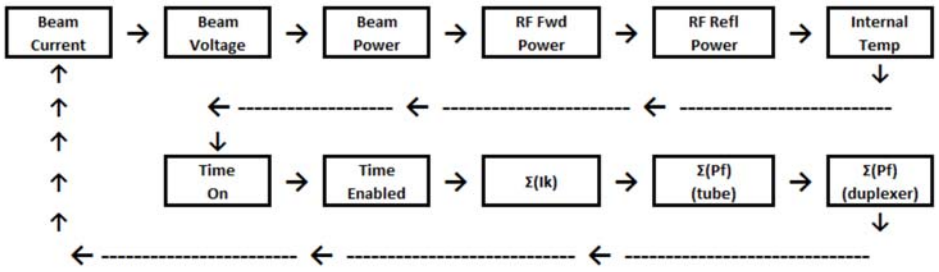
The front panel of the TPS02 has a 4-line x 20 character LCD display. With the adjacent rotary encoder knob, the user modified the display, or reviews and modifies setup parameters. This section describes the original first build of the TPS02 – features may be modified for different customer specifications.

5.1 Top Level Displays

The "top level" of displays is selected by rotating the encoder. This will cycle through the options for display shown here:

For these top-level displays, the display is in a 3-line mode with a double height center line. The center line shows the current value of the parameter being displayed, as in the example at right. The bottom line is unrelated to this parameter, but instead gives information on current status.

Figure 6. Top level display shows one of several parameters, and the system status in the lower right corner.



5.1.1 Status Line

The status line gives the current status of the TPS02, in the following hierarchy:

"Interlock Open" - if the hardwired interlock is broken; else
"EStop" - if the EStop button on the front panel is activated; else
"Xfault" - if a fault extreme enough to open the breaker is activated (i.e. Ik interpulse); else
"Hfault" - if a hard fault has latched (i.e. Ik overcurrent); else
"Pulsing" - if HV or RF have pulsed in the previous second; else
"Enabled" - if the TPS02 is enabled to pulse but has not pulsed in the last second; else
"Breaker" - if the TPS02 has permitted the PLC to close the facility breaker; else
"Idle" - otherwise.

5.1.2 Top Level Display Details

Beam Current – This displays the digitized output of the sample/hold amplifier on the Ik channel[7]. The S/H is gated during the HV pulse, and there is a 3 µs *RC* filter between the S/H amp and the digitizer, so this display will typically show the average over the last few micro-seconds of the latest pulse. *For this reason, the current will not display accurately for very short beam pulses (i.e. less than ~5 µs).* The absolute calibration is dependent on the accuracy of the current transformer, with 1% components in between. The value is displayed in units of Amps with 100mA resolution.

Beam Voltage – This displays the digitized output of the sample/hold amplifier on the Vk channel[7], similarly gated and filtered, and with similar cautions for short pulsewidths. The absolute calibration here is derived from the compensated voltage divider, and the value is displayed in units of kV, with 100V resolution.

Beam Power – This displays the calculated beam power, simply the multiple of the Klystron Voltage and Current, discussed above.

RF Forward Power – This displays the diode detector signal for RF channel #0 forward power[8]. Unlike the current and voltage, this sample/hold amp is gated during the RF pulse rather than the HV pulse. There is a similar 3 µs *RC* filter on this channel, thus with similar cautions for short RF pulsewidths. The absolute calibration is dependent on the calibration coefficients loaded by the user into the TPS02. The value is displayed in units of kWatts, with 1 kW resolution.

RF Reflected Power – This displays the diode detector for RF channel #0 reflected power. Processing is identical to the forward power.

Internal Temperature – This shows the temperature inside the TPS02 unit. This should be checked occasionally, especially if operated in a high temperature environment, and additional cooling or air flow provided if the temperature is excessive.

[7] The S/H amps do not hold well for long time periods (i.e. minutes). If no pulses are detected in the last 5 seconds, the S/H amps will be briefly gated to zero the hold values at 5 second intervals.
[8] RF channel #0 has additional instrumentation that is not provided for the other directional coupler channels, and should be used for the first directional coupler after the Klystron.

Time On – This is one channel of the "odometer" functionality of the TPS02. This is an accumulated timer that shows total time that the TPS02 is powered up. The value is kept in units of seconds on a 32 bit counter, thus having a range of over 136 years. The units shown vary depending on the value, from seconds to khrs, with decreasing resolution as the duration is increased. This value can also be extracted *via* serial interface, and can never be re-zeroed.

Time Enabled – This odometer channel shows the accumulated time during which the TPS02 is "running"...i.e. enabled to pulse. Display formatting is same as for Time On. This value can also be extracted *via* serial interface, and can be re-zeroed and thus used as a measure of tube lifetime. Re-zeroing cannot be done over the LCD/rotary encoder interface, and must be done over serial (see Section 6.7.5).

Σ(Ik) – This odometer channel displays the integrated current through the klystron. It is updated at the falling edge of every HV pulse, and incremented by the HV pulsewidth multiplied by the most recent S/H Klystron Current reading. This is accumulated in 64-bit storage in non-volatile memory. The display reads only the top word of this, and is displayed in kC, MC, or GC depending on the value. The range before overflow is >500 GC, which is over 1700 years of 24/7 operation at full current and duty. This value can be extracted *via* serial interface, and represents the tube life. It can be re-zeroed with tube change, but this cannot be done over front-panel operations and must be done over serial interface (see Section 6.7.5).

Σ(Pf) – total – This odometer channel displays the integrated RF power through the Klystron. It is updated at the falling edge of every RF pulse, and incremented by the RF pulsewidth multiplied by the most recent S/H RF Forward Power reading. It is important to note that the accumulated value is dependent on the diode calibration curves at the time of accumulation – changes in calibration curves at a later time will not adjust the historical sums.

The value is accumulated in 64-bit storage in non-volatile memory. The display reads only the top word of this, and is displayed in MJ, GJ, or TJ depending on the value. The range before overflow is > 4500 TJ, which is nearly 300 years of 24/7 operation at max power and duty. This value can be extracted *via* serial interface, and also represents the tube life. It is also re-zeroed with tube change, which must be done over serial interface (see Section 6.7.5).

Σ(Pf) – duplexer – This odometer channel is identical to the one above, except that it only accumulates when the waveguide switches are set to "antenna" rather than to "dummy load". This is intended to be a separate measure of duplexer lifetime, and is separately re-zeroed using a different command than that for the tube-change (see Section 6.7.6). Scaling and rollover are identical to that of the previous channel. This can be extracted *via* serial.

5.2 Display Setup Menus

The display and rotary encoder are used to enter the setup menus, where various parameters may be reviewed and changed. All of these setup parameters are also accessible *via* serial interface, and it is expected that most of these will regularly be entered by that route using automated scripts, rather than painfully entered manually on this user interface[9].

The lower tiers of the display menus can be entered ***WHEN THE TPS02 is NOT ENABLED for pulsing ONLY.*** This is done by ***pressing*** the rotary encoder rather than rotating it. If the encoder knob is pressed while the TPS02 is enabled, an error message will result.

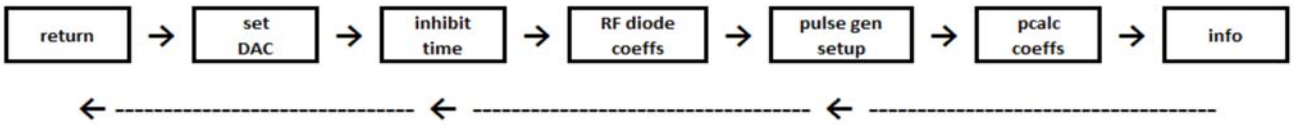
Properly entering the setup menus will allow you to work through the hierarchy shown below. At any point, if there is no activity for several seconds (press or rotation), the interface will time out and return to the top tier at the Klystron Current display. Alternately, there is a "return" selection at each sub-menu, which will return up one level. Returning from the 2nd tier will always return to the top tier displays at Klystron Current.

At any point while traversing the menu tree, you can rotate the encoder or press the encoder. At any of the branches on the menu tree, you are selecting among other sub-menu choices, and the rotary encoder will cycle through these choices (one of which will be highlighted between brackets, i.e. "»return«"). Pressing will branch off up or down accordingly.

At the terminal nodes of the menu tree, you are not selecting among sub-menu choices, but are instead reviewing and modifying a parameter. In that case, the present value of this parameter will be displayed, and a modified value displayed below it. Spinning the encoder will increase or decrease the modified value, and pressing the encoder will lock in the modified value.

"Locked in" values are held in sram (volatile memory) until the return to the top-tier menus, at which point the entire parameter block is copied over to flash (non-volatile) memory.

5.2.1 Tier 2 sub-menu



The tier 2 sub-menu selects among the primary setup categories for the TPS02.

set DAC – There are 32 12-bit digital-to-analog converters in the TPS02. Most of these are used to set fault comparator thresholds. Spares are bypassed by these menus and require firmware update to include in panel controls. DAC setpoints may also be examined and set *via* the serial interface.

inhibit time – There are 11 inhibit timing channels used to suppress fault responses during transitions (i.e. "rabbit ears" or "cable charging currents"). These have pre-defined functions in

[9] Naturally, the syntax is vastly different for the two interfaces. The display interface is wordy, and built for review and entry using a rotary encoder only. The serial interface is terse, dense, and often hexadecimal – it can be used with a keyboard and terminal emulator, but is intended for computer-to-computer use.

the firmware (i.e. leading or trailing edges, HV pulse or RF pulse edges, and which comparator faults are inhibited), but the menus allow the delay times to be modified. Timer setpoints may also be examined and set *via* the serial interface.

RF diode coefficients – There are many different RF diode channels processed in the TPS02, but only channels processed in the four control board analog processing channels are calibrated. Typically this is done for one RF directional coupler, forward and reflected power – and it is these two channels which show calibrated display values, and one of which is used for the odometer integrated power accumulator. These two channels are calibrated with a zero intercept 2nd order polynomial, thus there are four coefficients (two each) that are loaded here to determine these calibrations. Diode Calibration coefficients may also be examined and set *via* the serial interface.

pulse generator setup – The TPS02 has an internal pulse generation function for testing and tube conditioning. The choice of external (radar) beam and RF pulse requests *vs.* internal pulse generator pulse requests is made *via* a control bit from the PLC. The PLC may also select one of sixteen pre-set test patterns using a 4-bit code. Each test pattern is defined by PRF, beam pulsewidth, RF pulsewidth, and beam-to-RF delay time. There are thus 64 parameters to load to define all of these presets. Use of the Pulse Generator is not allowed while the waveguide switch bits from the PLC indicate radiation out of the radar antenna – the waveguide switch must indicate transmission to the dummy load for Pulse Generator use. The Pulse Generator entries may also be examined and set *via* the serial interface.

Pcalc Coefficients – The TPS02 performs two realtime tests of klystron output power, comparing to pulsed beam power, and alerting the transmitter team if the RF power appears low. One of these is in hardware, and uses two DAC coefficients described in the next section. The other is more accurate, but slower, and is calculated by the CPU at regular intervals from the S/H values of I_k, V_k, and P_{f0}. That calculation needs two coefficients: the presumed power efficiency of the Klystron and an offset to avoid nuisance faults.

info – this is a documentation screen, which simply displays the firmware version and build date.

5.3 Tier 3 sub-menu – "set DAC"

This sub-menu cycles between all DAC channels which are in use. The DAC setpoints may also be examined and set *via* the serial interface. Detailed discussion of specific channels are omitted for this generic manual. Typical channels specify the fault overcurrent levels, fault reflected RF power levels, interpulse fault levels of current or voltage, etc.

5.4 Tier 3 sub-menu – "Inhibit Time"

The TPS02 has eleven inhibit timer channels available. These are generated using internal clocks in the control board CPU, and subject to the constraints of these clocks. (The Timer setpoints may also be examined and set *via* the serial interface.) Detailed discussion of specific channels are omitted for this generic manual. Typical channels are dedicated to HV gate edges

(leading, trailing, or both); or RF gate edges (leading, trailing, or both), and allocated to specific fault comparators to inhibit faults during transients.

5.5 Tier 3 sub-menu – "Diode Calibration Coeffs"

This menu cycles between the coefficients used to give a polynomial calibration curve for the RF detectors assigned to any of the four control board analog channels. Specific details are implementation dependent, and omitted here.

5.6 Tier 3 sub-menus – "Pcalc Coefficient Setup"

The TPS02 performs two realtime checks of RF power *vs.* I_k*V_k. One of these is calculated in the CPU using the calibrated diode power, thus this is more accurate than the hardware check which has a linear approximation. For this calculation, the minimum RF expected is calculated like so:

$$P_{RF\text{-}min} = I_k * V_k * eff - P_{offset} \quad ,$$

and is compared to the most recently sampled RF power.

There are two entries under this sub-menu: Efficiency and Power Offset. The Efficiency is entered in percent, and power offset entered in kW.

The Pcalc coefficients may also be read and set using the serial interface. Detailed discussion of this calculation is in Section 8.0.

5.7 Tier 4 sub-menus – "Pulse Generator Setup"

The TPS02 has an internal pulse generation function for testing and tube conditioning. The choice of external (radar) beam and RF pulse requests *vs.* internal pulse generator pulse requests is typically made *via* a control bit from the PLC. The PLC may also select one of sixteen pre-set test patterns using a 4-bit code. Each test pattern is defined by PRF, beam pulsewidth, RF pulsewidth, and beam-to-RF delay time. There are thus 64 parameters to load to define all of these presets. The Pulse Generator entries may also be examined and set *via* the serial interface.

To aid ergonomics, we insert an extra tier here – the level 3 sub-menu has seventeen choices: return and pulse-generator-channel-X, for X given values of 0-15.

Selection of any pulse generator channel brings you to a 4th level sub-menu dedicated to that channel with only five choices: **return, PRF, HV pulsewidth, RF pulsewidth, and dT.** The PRF and pulsewidths are self-explanatory, and the ***dT*** setting is used to set the delay between the leading edge of the HV pulse and the leading edge of the RF pulse. Further details omitted here.

6.0 Serial Interface

A serial port is provided for remote configuration and inquiries which are more complex than the PLC interface is capable of. This port uses two 5 MBaud ST type transmitter/receivers and multimode 62.5/125 μm fiber, with transmission ideally capable of over 1 km paths. The serial communications are set for 115200 Baud, 8 bit, no parity.

6.1 Ergonomics

The serial port is *intended* to be operated by a remote computer running scripts. To that extent, the commands are simple and terse, and the replies are minimal and terse. Requests for data, for example, are replied to with the appropriate number only, no header or units. Data will generally be presented without stripping leading zeros, and must always be entered will all significant figures specified as well (the LCD display, in contrast, does strip leading zeros).

The serial port *may be* operated, however, by a user at a terminal. To that extent, all commands and replies are formatted in readable ASCII characters and properly separated by <CR><LF> terminations.

If using the serial interface with a terminal emulator and a human, keep in mind that the help menu shown on the previous page is accessible by typing a question mark "?" followed by carriage return, <CR>. It has terse but understandable syntax instructions for all of the commands listed below.

6.2 Flash Memory

All parameters are generally kept in volatile sram (static ram). This sram is loaded at boot-up from the non-volatile flash memory on the TPS02.

The front panel user is assumed to be inattentive or unintelligent (vastly different but often with similar consequences). We thus take liberties and make assumptions for this user. One important liberty we take is that changes that the front panel user makes, although changed to sram, are copied to flash immediately upon returning to the top-tier display.

Not so with the serial interface. We do wish to conserve flash write events, as the flash is only specified for a finite number of write cycles (not to worry too much, this is ~100,000). The serial interface user ***ONLY*** changes the sram mirror until s/he specifically instructs the TPS02 to copy the sram to non-volatile flash. We assume that the serial interface user is both intelligent and attentive enough to make all desired changes to parameters followed by a single copy to flash command.

6.3 Serial Comm is not Locked Out

We noted above (Section 5.2) that the lower tiers of the LCD Display menus are *not* accessible when the TPS02 is enabled for pulsing. This is out of an abundance of caution, particularly to avoid changing parameters during pulsing activities where the results may be unpredictable.

We have opted not to enforce this lockout for Serial Communications. It is anticipated that the user of the serial interface will be more cautious, and likely will be scripted / autonomous which is properly synchronized with the PLC to only make changes when not enabled.

It should be noted that all critical CPU functions during pulsing (generation of inhibit timing signals and event logging) are interrupt driven, and latency is unlikely to be increased by keeping the CPU busy with serial communications – however caution is always prudent with sensitive equipment, and it is suggested that the user minimize serial comm while ENABLED.

In particular, while serial information interrogations are likely harmless, parameter changes during pulsing may cause unpredictable results. Extensive debugging experimentation showed the TPS02 system to be quite robust in this regard, but caution is advised. Some features of violating this rule were observed – such as changes to pulse generation setup parameters while pulsing are not implemented until the next time the clock counters are loaded – which requires the ENABLE bit to be cycled off then on. Rather than document all these features, we simply suggest... don't do it. If requested, we may implement a serial comm lockout while enabled on future firmware revisions.

6.4 Serial Information Requests

There are three "information request" commands available on the serial port. These are intended for the human interfacing via a terminal. These requests are:

"?" - help menu, lists all commands and *very* brief descriptions
"R" - **R**emind us of DAC channel assignments (table below)
"P" - **P**lease remind us of Timer channel assignments (table below).
"X" - Show the version number and build date of the firmware.

6.5 Serial Inquiries

A large number of inquiries exist for extracting information out of the TPS02 *via* the serial interface. Omitting the formatting details, these are:

"vdc" - Read a DAC setpoint (read voltage on DAC device "d" sub-channel "c")

"tdc" - Read a Timer setpoint (read timer setting on device "d" sub-channel "c")

"cd" - Read Diode calibration coefficient (coefficient "d")

"wc" - Read Pcalc coefficient (channel "c")

"gcf" - Read a Pulse Generator table entry (channel "c", function "f")

"n" - Read the number of events in the event-logger memory

"d" - Read a dump of a block of up to 64 events (each event is formatted in a 25 byte string, with an index number, a 12-character hex bit pattern, and an 8-character hex timestamp)

"x" - Read all fault bits (returns an 8 character hex string reporting all fault bits)

"y" - Read all "first-latched-fault" bits (returns an 8 character hex string for all bits).

In addition, there are specific commands to request the current reading of any of the digitized analog values, the TPS02 internal temperature, and the "odometer" time, integrated power, and integrated current logs.

6.6 Serial Parameter Settings

There are a similar set of commands to *set* parameters over serial. Most of these are nearly identical to the corresponding inquiries in the previous section with the following differences: The command character is upper case instead of lower case, and the command format is extended to include the value to set. Omitting specific formatting details, these are:

"Vdcnnn" - Set a DAC setpoint (set hex "nnn" to DAC device "d" sub-channel "c")

"Tdcnnn" - Set a Timer setpoint (set hex "nnn" to timer device "d" sub-channel "c")

"Cdnnn" - Set a Diode calibration coefficient (set hex "nnn" to coefficient "d")

"Wcnnn" - Set a Pcalc coefficient (set hex "nnn" to channel "c")

"Gcfnnn" - Set a Pulse Generator table entry (set hex "nnn" to channel "c" function "f")

6.7 Serial Actions

There are several serial commands which perform actions distinct from setting values of parameters. These are itemized here:

6.7.1 "Q" – Write SRAM to FLASH

The non-volatile flash memory in the TPS02 is infrequently accessed, as it is a slower external interface than the internal (volatile) SRAM within the processor. The flash is separated into parameter space and history space, and both are read into SRAM mirrors at boot-up time. The mirror space is accessed frequently during operation, and the history block continuously updates the odometer accumulators. The SRAM mirrors are written back to flash at specific times – parameters are re-written whenever the front panel user returns from setup menus to top-level display. The history block is written to flash every time the ENABLED status drops (which includes any fault), and every 2.5 hours otherwise.

Command "Q" forces a flash write immediately of both history and parameters.

6.7.2 "S" – Start Event Logger

Command "S" clears the event counter and event memory, and starts the logger running. The logger will tag an event on any change of any of the designated bits, saving a snapshot of all designated bits and a timestamp.

6.7.3 "s" – Stop Event Logger

Command "s" stops the event counter from logging events, and initializes some parameters for subsequent readout of the logger memory. It is necessary to stop the logger before reading the logger memory.

6.7.4 "r" – Reset Faults

Command "r" performs a reset of all fault latches. Note that all fault latches can only be reset if the original fault condition is no longer the case – faults cannot be overridden by resetting. The operation of a reset over serial interface is identical to that performed by PLC or front panel pushbutton.

6.7.5 "Z" – Reset Tube Odometer Accumulators

Command "Z" resets the "tube life" odometer accumulators. These include the "enabled time", the "integrated beam current" and the "integrated total RF power".

This reset cannot be undone – and should be undertaken only after careful consideration. To avoid accidental reset, the reset must be validated by a subsequent "Y" entry.

A flash write is forced after the reset.

6.7.6 "z" – Reset Duplexer Odometer Accumulators

Command "z" resets the "duplexer life" odometer accumulator. This is the "integrated total RF power through antenna".

This reset cannot be undone – and should be undertaken only after careful consideration. To avoid accidental reset, the reset must be validated by a subsequent "Y" entry.

A flash write is forced after the reset.

6.7.7 "F" – factory reset parameters

The serial command "F" is provided to reset all user enterable parameters to the factory reset values.

7.0 Operation

With all interconnects to PLC, input pulse requests, pulse outputs, and diagnostic inputs properly hooked up, operation can commence.

The interlock should either be jumpered, or connected to user interlocks providing continuity to the two interlock pins.

The ESTOP should be released – this switch has a mechanical latch, and must be twisted to release if activated.

7.1 Sequencing

Sequencing is configuration dependent, and specific to each customer. Typically, a conversation will take place between the TPS02 and a facility PLC to sequentially increment the readiness of the transmitter.... this will include closing breakers, warming up supplies, checking facility services such as cooling and personnel interlocks, enabling power systems, and finally enabling the TPS02 to pass pulse requests to the HV modulator and RF gates.

7.2 External vs Internal Pulsing

With the PLC "pulse generator" control bit off, the pulse requests to the TPS02 will come from the external DTTL input port.

With the PLC "pulse generator" control bit on, the pulse requests are generated internally using the internal pulse generator. This will be "turned on" with the ENABLE signal.

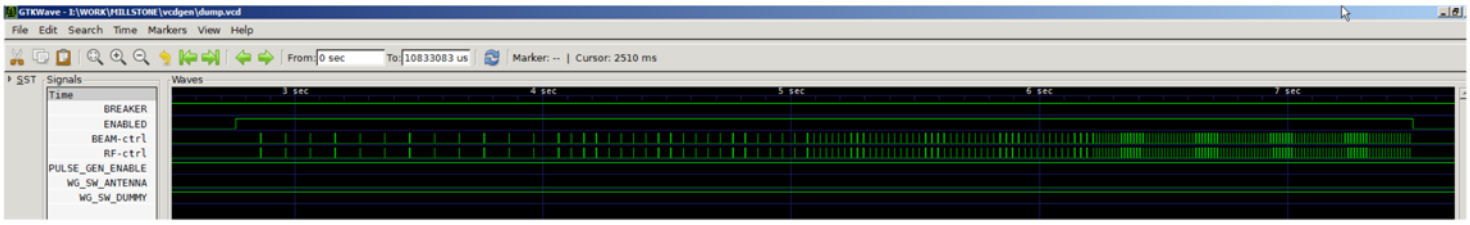
See Section 5.7 for instructions on setting up the Pulse Generator *via* the front panel menus. The Pulse Generator is activated by a PLC control bit, but operation is only allowed when the waveguide switch bits indicate that the klystron output is directed to the dummy load.

7.2.1 Hint for Tube Conditioning – Gray Code

The Pulse Generator, as specified, has 16 presets. Each preset can be set with unique values for PRF, beam pulsewidth, RF pulsewidth, and leading edge delay. It is intended that these can be used to gradually increase the duty cycle while conditioning a new klystron, or reconditioning after a particularly bad arc. The selection between the various presets can be made in "real time" by changing the 4-bit selection code from the PLC[10].

If these bits are set by manual switches, or if the PLC is particularly slow in response time, then intermediate states may cause unwanted high-duty transients during switching between two low-duty states. We recommend that such a gradual sequence be coded in "Gray Code", an alternate form of binary where only one bit flips at a time.

[10] The switches are re-sampled at the end of every HV pulse, and if they have changed since the previous pulse, the clock is stopped, reloaded, and restarted. Note that the exception to this is pulse gen state 0 (0000). The enable bit must be cycled to properly transition from single shot mode back to repetitive mode.



Example – The screen capture above is from a short sequence using the TPS02 pulse generator and the internal Event Logger (Section 9.0). The pulse generator was setup with a "tube conditioning sequence of 4 states. All four were set with HV pulsewidth of X µs, RF pulsewidth of X µs, and *dt* of X µs. In succession, state 1 (bit pattern 0001) was set to 10 Hz, state 3 (0011) was set to 20 Hz, state 2 (0010) was set to 40 Hz, and state 6 (0110) was set to 80 Hz.

The sequence consisted of rapidly flipping single switches to sequence between these states, and even zoomed out fully (the view is about 5 sec total), the increasing duty cycle can clearly be seen.

7.2.2 Single Shot Mode

The Pulse Generator has 16 presets. One of these, #0 or selection bit pattern 0000, is designated for single-shot testing, and hence has no PRF. The beam pulsewidth, RF pulsewidth, and leading edge *dt* are set up as usual, but pulses are generated one at a time by pressing the front panel "SS Pulse" button, or pulsing the associated PLC bit. One pulse only will be generated on each button press (the debounce time is quite long – 750 ms for both press and release).

7.3 Faults and Fault Reset

Faults are of several varieties. In order of severity, from less to more:

7.3.1 Warnings

Warnings are generated by mismatch between RF power and beam power, as discussed in Section 8.0 These warnings result in a flashing LED on the front panel (P_{f0} FLT) and a parallel bit to the PLC (presumably to flash an indicator on the operator's panel). Pulses are not interrupted, and the condition is not latched.

Warnings are also generated by pulse waveforms which exceed the allowed specifications for PRF, pulsewidth, duty fraction, deadtime, etc. These warnings similarly result in a flashing LED (PLSerr) on the front panel and a bit to the PLC. Again, the condition is not latched nor is pulsing inhibited, but the pulse waveform is adjusted to conform to specifications. For example, excessive pulse width will be truncated, and excessive PRF or duty will result in dropped pulses.

7.3.2 Soft Faults

Soft fault conditions are used for some systems to discriminate tube arcs from waveguide arcs. The latter – detected by excessive RF power or waveguide arc detectors – can be used to shut down RF without shutting down the beam. After a short (many ms) delay for arc clearing, the RF may be re-enabled. When used, additional parameter entries are added to the system to configure the restart delay and maximum number of restart tries.

7.3.3 Hard Faults

Hard Fault conditions are tube arcs or TPS internal errors. In systems without Soft Fault capability, the waveguide arcs and high reflected RF power faults are also Hard Faults.

Generally, interpulse leakage of RF forward power, which indicates klystron oscillation, is also considered a Hard Fault.

The internal errors which may cause Hard Faults include failure of any of the internal power supply rails (four tests performed on each board), as well as sequence faults.

All Hard Faults are latched, and result in immediate termination of both RF and BEAM output pulsing, by removal of the ENABLED state. The latches require a RESET to clear, and the reset will not be applied unless the fault condition itself is no longer present. If the PLC ENABLE REQUEST bit remains on, pulsing will immediately resume on clearing the fault latches.

Note that continually holding RESET will not present a "battle short" to ignore faults. Indeed, pulsing is inhibited while the RESET bit is on, and does not resume until it is released.

7.3.4 Extreme Faults

Extreme Faults are those which require immediate removal of mains power from the HV systems. These generally include ESTOP, Interlock break, and interpulse leakage of either I_k or V_k. Occurrence of an Extreme Fault will result in all the responses of Hard Fault, plus the release of the BREAKER bit, which should signal to the PLC to open the mains breaker.

7.3.5 Resets

Warnings auto-reset, as they are not latched. Hard Faults and Extreme Faults can be reset with the front panel Reset button, the PLC Reset bit, or the serial Reset command. No latched faults will reset if the condition persists. Operation is not permitted while the reset button (or bit) is held on.

8.0 RF Power Checks

The TPS02 performs two realtime checks of RF power *vs.* I_k*V_k. One of these is calculated in the CPU using the calibrated diode power, thus this is more accurate than the hardware check which has a linear approximation, however it is slower and prone to software risks. The other is performed entirely in hardware, hence it is faster and more reliable, but it is less accurate as it assumes a linear voltage-power relationship for the diode.

The response to a failure of *either* of these checks is determined by the user specification. This may generate a soft or hard fault, or may merely flash a warning bit to the PLC.

8.1 Calculated Check

For the calculated RF power check, the minimum RF power expected is calculated like so:

$$P_{RF\text{-}min} = I_k * V_k * eff - P_{offset} \quad .$$

If the RF forward power on channel #0, as sampled during the most recent pulse is less than this value, the test fails with the response discussed above.

The user may enter values for the expected klystron efficiency and the calculation offset by either the front panel menus (see Section 5.6) or by the serial interface.

8.2 Hardware Check

The hardware calculation of RF power uses DAC setpoints and two analog multiplier chips to effectively calculate a similar check electronically. First, the realtime (buffered and scaled) I_k and V_k signals are multiplied, generating a realtime signal representing beam power, scaled at 1.5 MW/V. This is present on the top (control) board on a testpoint, TP3, easily accessed with the top cover off.

We then multiply the beam power by a number similar to the efficiency above – we call this the gain. The range is 0-100%, and is set using one of the 12-bit DAC channels. We then subtract an offset voltage similar to above, to avoid nuisance faults (and to provide a margin for the linearization error). This has a range of 0-10V, and is set using another of the 12-bit DAC channels. After multiplying by the gain and subtracting the offset, this value is compared to the uncalibrated internal-bus value of the P_{f0} signal (which has a nominal range of 0-10V).

9.0 Event Logger

The TPS02 includes an event logger for use in capturing and inspecting the overview of the entire system during pulsing or faults. This system operates similarly to a logic analyzer – it monitors a number of digital signals and captures an "event" every time any of these signals change state. The data captured on an event includes a snapshot of each of the signals of interest, plus a timestamp. The event memory is 4096 events deep – if the memory exceeds this, it rolls around overwriting earlier data (similar to the capture memory in a digital storage scope waiting for a trigger).

The event logger is an independent and asynchronous tool built into the TPS02 – it does not start or stop automatically, but only under serial control. In this way, it can capture the sequence of state control bits that precede operation. There are no controls for the event logger accessible from the front panel interface – access to the logger is done *via* the serial port. Although all controls and readout of the logger use printable ASCII characters, the interface is really intended for control by a remote scripting computer over the serial port.

The response of the TPS02 to an "event" is triggered by any of the bits of interest changing state – all these bits are wired to pin-change-sensitive ports on the CPU and configured to generate an interrupt. The interrupt service first initiates any inhibit timers needed – since RF and BEAM gating edges are bits of event interest – thus the latency for logger sensitivity may be 4-5 µs in some cases. See Section 5.4 for a more complete discussion of the limits of accuracy of the inhibit timers – as this also applies to event logger snapshots.

9.1 VCD Format Files, GTKWAVE, and VCDGEN.exe Tool

Inspection of the data dumped from the Event Logger can be done by user-generated tools to interpret and plot the output data. In addition, there are standards for similar tools – including standards for data interchange files – available for use with third party tools.

These standards are discussed in the Wikipedia article on Waveform Viewers[11]. One of the prolific standards which is particularly suitable for our use is the VCD format (Value-Change-Dump). A very simple tool, VCDGEN, was written (for W7/64, using Lahey-Fujitsu Fortran) to do the following:

- Start the logger
- Wait for the user to hit <CR>
- Stop the logger
- Interrogate the logger for number of events
- Download all events
- Recast the event data into a VCD format file.

One tool from the Wiki article[11] that is both suitable for VCD and open-source was downloaded and installed – this is GTKWAVE. Although the format of the VCD files generated by VCDGEN cannot be guaranteed to be universal, it proves to be compatible with GTKWAVE,

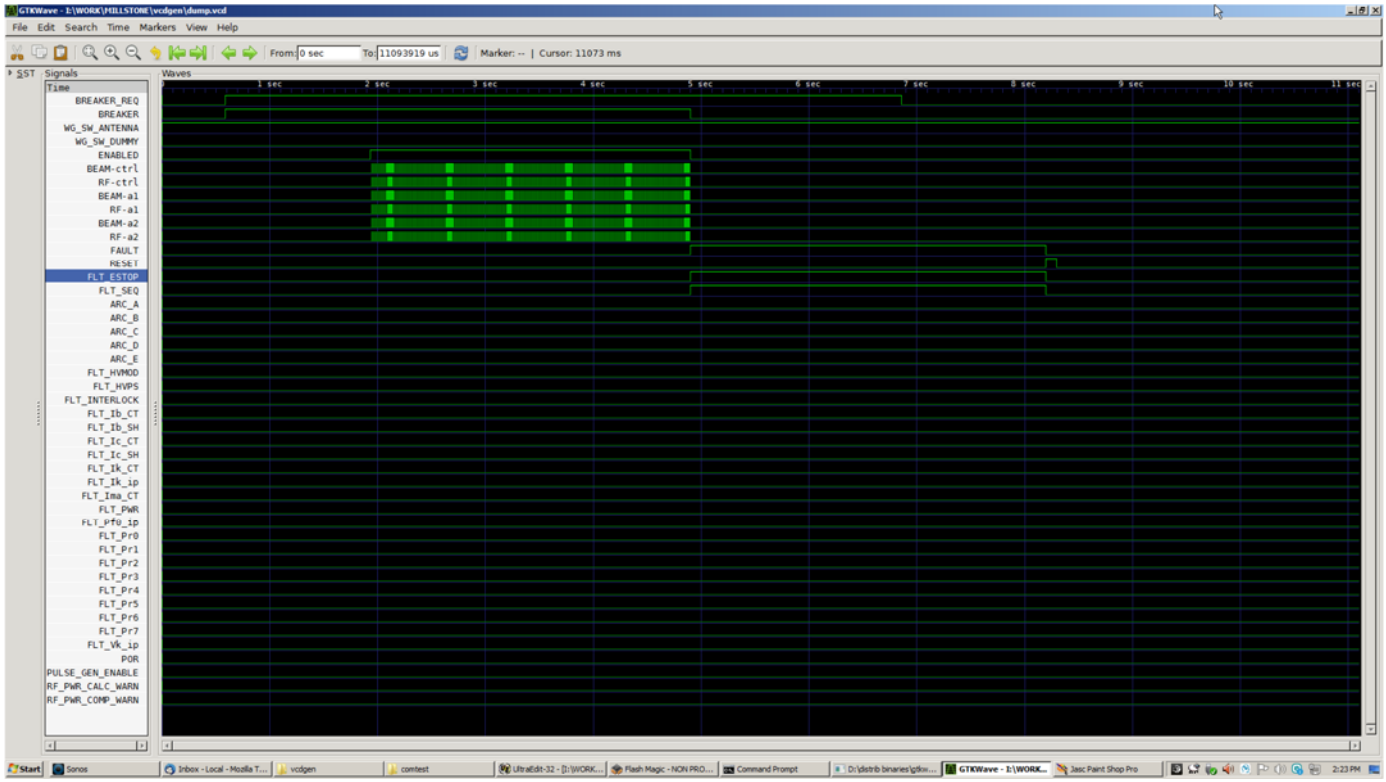
[11] See https://en.wikipedia.org/wiki/Waveform_viewer.

thus rendering it simple to generate visible plots of the TPS02 operation. The listing of VCDGEN is supplied (omitted here) as a template for the user to craft similar custom code.

9.2 Event Logger Example

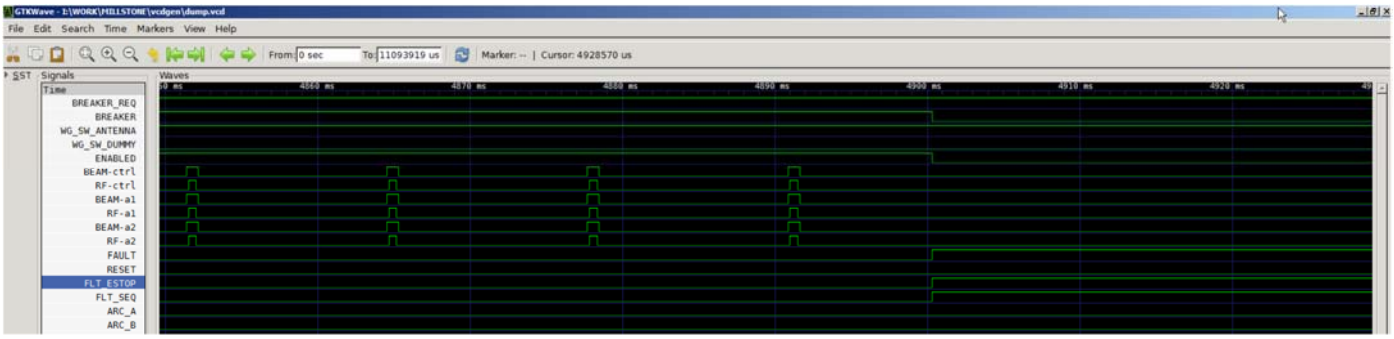
We set the TPS02 to run with external pulse waveforms, set to XX Hz PRF, about XX µs beam pulsewidth, about XX µs RF pulsewidth, and the RF pulse approximately centered in the beam pulse. We start the logger, then sequence through BREAKER and ENABLE status bits *via* the PLC – pulsing initiates after the ENABLE bit is turned on. After about 3 seconds, we hit the ESTOP to crash the system, then turn off the sequencing bits from the PLC and reset the latched fault.

We have the logger running through this sequence, and the first shot below is the fully unzoomed view in GTKWAVE of this data set (912 events total over about 11 seconds).



GTKWAVE allows us to arbitrarily shuffle the placement of the signals, so we have done so, putting the bits of interest near the top. Note that we are plotting three separate signals each for the BEAM and RF – we can use these in our custom code to ensure that we haven't lost synch between the data captures on the three boards.

Zooming in on the last few pulses before the ESTOP event, we now see about 80 ms worth of signals:



Further zooming in, to a window of about 1.1 ms surrounding a single pulse, we see the details of the beam and RF pulse timing (omitted).

10.0 Allocation of comparators and Inhibit timers

We have discussed comparators in use as we surveyed the above channels. There are additional comparators available for expansion.

Each analog board has feetprint for sixteen comparators – eight with DAC thresholds and eight with either pot or fixed resistor thresholds. There is a vast array of 0603 resistor placements which can be used to connect these to any of the sixteen analog-bus signals (within certain limits) which result after the initial input buffering and scaling. To use these, the parts must be populated and the connection made, usually with the 5kΩ resistor which constitutes the *R* of the *RC* filter at the signal input to the comparator.

The analog board #1 (middle board) has 13 of 16 presently in use. Of the three spares, one has a DAC threshold reference. These are shown along the bottom of page 5 of the schematic.

The analog board #2 (lower board) has 7 of 16 presently in use. Of the nine spares, three have DAC threshold references, scattered numerous places in the schematic.

The control board (top board) has patterns for thirteen comparators, eleven with DAC thresholds, one with a pot-reference, and one with fixed reference. Of these, four with DAC thresholds are spares.

11.0 Reprogramming

There are multiple programmable chips in the TPS02. Bug fixes or spec changes will require updating the firmware. This is easily done with a Windows computer and a USB cable (included). **This USB cable should only be used for reprogramming, disconnected otherwise.**

The top board (control board) has an ARM7 embedded processor, which controls most of the user ergonomics and some system state functions, as well as generating all comparator inhibit timing and event logging. Each of the two analog boards has a lesser ARM7 processor – these act as slaves to the control board, and have far fewer functions (namely archiving logged events for signals on the local board, and acting as a programming interface for the CPLDs).

In addition, the fast fault logic and critical state functions are handled by the fast CPLDs[12] on each board – two on the control board and one each on the analog boards.

Reprogramming the CPUs is done directly by connecting the USB cable to the appropriate port on the rear panel and to a PC, and running the 3rd party tool provided for NXP ARM7 users – Flashmagic. Reprogramming the CPLDs is done *through the CPUs* over the same USB cable. For this purpose, each CPU has embedded code to drive the reprogramming, and we provide a Windows interface which communicates with the CPU over the USB cable to download the CPLD chip image and script the programming.

There are many steps to this process, each is described in detail below – however the user should not be intimidated. Once setup properly, firmware upgrades to either CPUs or CPLDs are simple and reliable.

New for 2018 – a new boardset, TPS02.2, now requires only a single USB port on the back panel, reducing confusion by the user. All programming is routed through the control board in this case. The TPS02.2 boardset is otherwise functionally equivalent in all other features.

Sections below (omitted here), detail the necessary USB drivers needed on the mating computer to communicate with the TPS02, as well as the specific tools supplied and instructions for reprogramming any of the CPU or CPLD firmware in the TPS02.

12.0 Disassembly and Reassembly

Detailed instructions and photos omitted.

13.0 PLC Interface

The TPS02 has three SCSI68 type connectors for communication to a facility PLC. Detailed pinouts and functional scaling tables are omitted.

[12] CPLD – Complex Programmable Logic Device. A CPLD is similar to a PAL or FPGA, and has levels of complexity which just about split the difference.

14.0 Table of Analog Signals

Tables below (omitted) give all gain, filter time, comparator allocation, and logic responses for all analog channels of the TPS02.

15.0 Factory Defaults of Parameters

The table below (omitted) shows all parameters and reset values for the TPS02 control.